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**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

Application Number: 09/285,899
Filing Date: April 08, 1999
Appellant(s): YAMAZAKI ET AL.

Eric Robinson
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed July 10, 20066 appealing from the Office action mailed April 10, 2006.

**(1) Real Party in Interest**

A statement identifying by name the real party in interest is contained in the brief.

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of Claims**

The statement of the status of claims contained in the brief is correct.

**(4) Status of Amendments After Final**

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

**(5) Summary of Claimed Subject Matter**

The summary of claimed subject matter contained in the brief is correct.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

**(7) Claims Appendix**

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(8) Evidence Relied Upon**

| | | |
|---|---|---|
| 5227900 | INABA ET AL | 7-1993 |
| 5055899 | WAKAI ET AL | 10-1991 |
| 6141174 | TAKESHITA ET AL | 6-1996 |

**(9) Grounds of Rejeetion**

The following ground(s) of rejection are applicable to the appealed claims:

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9-16, 21-24, 33-36, 50-52, 54 and 57-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inaba (US 5227900) in view of Takeshita (JP 61-141174) and Wakai et al (US 5055899).

Inaba discloses all except for a leveling (organic resin) layer on the TFT and the pixel electrode on the leveling layer. See other detailed explanations in the office action mailed 06-05-01, if needed.

Takeshita teaches that the use of leveling film of organic resin over the TFT for an active matrix substrate is common (an usual way) in the art. Wakai discloses (see Figures 1-2) that a conventional active matrix substrate comprising a thin film transistor having a pixel electrode directly connected to the drain electrode suffers several disadvantages such as short-circuiting,

thus, it is hard to obtain a TFT which can stably operate without causing a short-circuiting between the pixel electrode and the drain electrode (see col. 2, lines 18-27, lines 63-68; Inaba discloses this similar conventional structure of having the pixel electrode directly connected to the drain electrode). Wakai solves the short-circuiting problem by forming the insulation/leveling layer (e.g., organic resin) between the pixel electrode and the drain electrode, wherein the pixel electrode is electrically connected to the drain electrode through a contact hole of the insulation layer. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ an insulating/leveling layer having a contact hole and formed between the pixel electrode and the drain electrode for avoiding disadvantages including short-circuiting, i.e., a leveling (organic resin) layer on the TFT and the pixel electrode on the leveling layer, as taught by Takeshita and Wakai.

**(10) Response to Argument**

Applicant's arguments are as follows:

(A) Request for consideration of Information Disclosure Statements.

(B) The present claims are not prima facie obvious based on the combination of Inaba (US 5227900) in view of Takeshita (JP 61-141174) and Wakai (US 5055899), i.e., the Office Action has not established a prima facie case of obviousness (three basis criteria steps have not been met) based on the following arguments:

(B1) Inaba fails to disclose the pixel electrode electrically connected to the TFT/semiconductor element through an opening formed in the organic resin/leveling film.

(B2) Takeshita (the secondary reference) appears to teach the TFT substrate for the solid state image pickup device, and thus the device in Takeshita would not able to incorporate in the device of Inaba, (the main reference, the display device being a liquid crystal display device and also employing ferroelectric liquid crystal material).

(B3) Takeshista fails to provide a proper motivation.

(B4) Inaba (published in 1993) was aware to the teachings of Takeshita (published in 1986). If it were important to have leveling layer in a liquid crystal display device, particularly one formed between a TFT and pixel electrode, then why is Inaba as silent as to the importance of such feature? Thus, it was not obvious at the time of the invention that it would have been desirable to provide a liquid crystal panel with a leveling layer formed between a TFT and a pixel electrode of the liquid crystal panel.

(B5) Wakai fails to disclose the leveling layer, rather discloses an insulating layer.

(B6) Inaba (the main reference) does not seem to be concerned with the short-circuiting problem that device of Wakai (the secondary reference). Thus, there is no reason to combine Wakai to the device of Inaba.

Examiner's responses to Applicant's arguments are as follows:

(A) Initialed IDS copies are enclosed.

(B1) The rejection is under 35 USC 103, not 35 USC 102. Inaba, the main reference, discloses the claimed invention except for the pixel electrode electrically connected to the TFT/semiconductor element through an opening formed in the organic resin/leveling film, as noted in the office action. The office action relies on the secondary references (Takeshita and Wakai) to teach this limitation that lacks from Inaba. Takeshita teaches that the use of leveling

film of organic resin over the TFT is common (an usual way) in the art. Further, Wakai discloses (see figures 1-2) that an active matrix substrate comprising a thin film transistor having a pixel electrode directly connected to the drain electrode suffers several disadvantages such as short-circuiting, thus, it is hard to obtain a TFT which can stably operate without causing a short-circuiting between the pixel electrode and the drain electrode (see col. 2, lines 18-27, lines 63-68; Inaba discloses this similar conventional structure of having the pixel electrode directly connected to the drain electrode). Wakai solves the short-circuiting problem by forming the insulation layer (e.g., organic resin) between the pixel electrode and the drain electrode, wherein the pixel electrode is electrically connected to the drain electrode through a contact hole of the insulation layer.

(B2) Takeshita discloses an active matrix substrate comprising a transparent substrate, a TFT formed on the transparent substrate including elements such as gate electrode, gate insulator, channel region, source and drain electrodes, an insulator formed on the TFT, a pixel electrode formed on the insulator. This is a common active matrix substrate for a liquid crystal display device (see at least Wakai, Figure 3). TFTs are merely used as driving switching-elements that individually drive pixel electrodes in any liquid crystal display device including twisted nematic LCD device, ferroelectric LCD device.

(B3) Takeshita teaches that the use of leveling film of organic resin over the TFT is common (an usual way) in the art. Further, Wakai discloses (see figures 1-2) that an active matrix substrate comprising a thin film transistor having a pixel electrode directly connected to the drain electrode suffers several disadvantages such as short-circuiting, thus, it is hard to obtain a TFT which can stably operate without causing a short-circuiting between the pixel electrode

and the drain electrode (see col. 2, lines 18-27, lines 63-68; Inaba discloses this similar conventional structure of having the pixel electrode directly connected to the drain electrode). Wakai solves the short-circuiting problem by forming the insulation layer (e.g., organic resin) between the pixel electrode and the drain electrode, wherein the pixel electrode is electrically connected to the drain electrode through a contact hole of the insulation layer. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ an insulating layer (organic resin) having a contact hole and formed between the pixel electrode and the drain electrode for avoiding disadvantages including short-circuiting, i.e., a leveling (organic resin) layer on the TFT and the pixel electrode on the leveling layer.

(B4) The comparison between the main reference's date and the secondary reference's date is irrelevant under 35 USC 103. The main and secondary references each provides a date that is prior to the effective filing date of the application, thus constitutes as prior art. The main reference(Inaba) discloses the claimed invention except for the pixel electrode electrically connected to the TFT/semiconductor element through an opening formed in the organic resin/leveling film, as noted in the office action. The office action relies on the secondary references (Takeshita and Wakai) to teach this limitation that lacks from Inaba.

(B5) Wakai discloses the insulating film 108 filling recesses generated upon formation of the above thin films and *flatten* (level) the surface above the insulating substrate (see at least col. 4, lines 52-54).

(B6) In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some

teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Takeshita teaches that the use of leveling film of organic resin over the TFT for an active matrix substrate is common (an usual way) in the art. Wakai discloses (see Figures 1-2) that a conventional active matrix substrate comprising a thin film transistor having a pixel electrode directly connected to the drain electrode suffers several disadvantages such as short-circuiting, thus, it is hard to obtain a TFT which can stably operate without causing a short-circuiting between the pixel electrode and the drain electrode (see col. 2, lines 18-27, lines 63-68; Inaba discloses this similar conventional structure of having the pixel electrode directly connected to the drain electrode). Wakai solves the short-circuiting problem by forming the insulation/leveling layer (e.g., organic resin) between the pixel electrode and the drain electrode, wherein the pixel electrode is electrically connected to the drain electrode through a contact hole of the insulation layer. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to employ an insulating/leveling layer having a contact hole and formed between the pixel electrode and the drain electrode for avoiding disadvantages including short-circuiting, i.e., a leveling (organic resin) layer on the TFT and the pixel electrode on the leveling layer, as taught by Takeshita and Wakai.

The office action has been established a prima facie case of obviousness (three basis criteria steps have been met), as explained above, and thus the present claims are prima facie obvious based on the combination of Inaba (US 5227900) in view of Takeshita (JP 61-141174) and Wakai (US 5055899).

**(11) Related Proceeding(s) Appendix**

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

TOANTON
PRIMARY EXAMINER

December 20, 2006

Conferees:
Dave Nelms, Supervisory Primary Examiner 2871
Ricky Mack, Supervisory Primary Examiner 2873

| Form PTO-1449 (Rev. 8-83) | U.S. Department of Commerce Patent and Trademark Office | Atty. Docket No.: 0756-1950 | Serial No. 09/285,899 |
|---|---|---|---|
| **INFORMATION DISCLOSURE STATEMENT** #9 (Use several sheets if necessary) | | Applicant: Shunpei YAMAZAKI et al. | |
| | | Filing Date: April 8, 1999 | Group: 2871 |

**U.S. PATENT DOCUMENTS**

| Examiner Initial | | Patent Number | Issue Date | Patentee | Class | Subclass | Filing Date (if approp.) |
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**OTHER DOCUMENTS** (Including Author, Title, Relevant Pages, Date, Place of Publication)

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| | | Wolf et al., Silicon Processing for the VLSI ERA, Lattice Press, Volume 1, 1989, pages 151-154 |
| | | Wolf et al., Silicon Processing for the VLSI ERA, Lattice Press, Volume 2, pages 66-72 |
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| Examiner | Date Considered 12/6/00 |
|---|---|

*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.